ATTORNEY DOCKET NO.: R. ADDINALL 1-1 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellants:	Ross Addinall, *et al.*
Serial No.:	09/639,288
Filed:	August 15, 2000
Title:	INTEGRATED CIRCUIT DIE FOR WIRE BONDING AND FLIP-CHIP MOUNTING
Grp./A.U.:	2814
Examiner:	Phat X. Cao

Commissioner for Patents
Washington, D. C. 20231

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ATTENTION: Board of Patent Appeals and Interferences

Sirs:

APPELLANTS' BRIEF UNDER 37 C.F.R. §1.192

This is an appeal from a Final Rejection dated June 4, 2002, of Claims 1-4 and 7-10. The Appellants submit this Brief in triplicate as required by 37 C.F.R. §1.192(a), with the statutory fee of $320.00 as set forth in 37 C.F.R.§1.17(c), and hereby authorize the Commissioner to charge any

additional fees connected with this communication or credit any overpayment to the Deposit Account No. 08-2395.

This brief contains these items under the following headings, and in the order set forth below, in accordance with 37 C.F.R. §1.192(c):

I. REAL PARTY IN INTEREST

II. RELATED APPEALS AND INTERFERENCES

III. STATUS OF CLAIMS

IV. STATUS OF AMENDMENTS

V. SUMMARY OF THE INVENTION

VI. ISSUES

VII. GROUPING OF CLAIMS

VIII. SUMMARY OF REFERENCES RELIED ON BY THE EXAMINER

IX. APPELLANTS' ARGUMENTS

X. APPENDIX A - CLAIMS

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is the Assignee, Agere Systems Guardian Corp.

II. RELATED APPEALS AND INTERFERENCES

No other appeals or interferences will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1-12 are currently pending in the application. The Examiner has indicated that Claims 11 and 12 are allowed, and that Claims 5 and 6 would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

IV. STATUS OF THE AMENDMENTS

The Examiner mailed a Final Office Action on June 4, 2002, rejecting Claims 1-4 and 7-10. In response, the Appellants filed an Amendment under 37 C.F.R. § 1.116 on August 1, 2002, in which the only proposed amendment included adding the word "only" to Claim 1. The amendment was proposed solely as clarification of the existing claim language, and did not add new subject matter. The Examiner mailed an Advisory Action on August 26, 2002, indicating that the amendment and arguments of the Amendment under 37 C.F.R. § 1.116 did not place the Application in condition for allowance. Moreover, the Examiner did not enter the amendment, and instead asserted that the amendment raised new issues that would require further consideration and/or search. Accordingly, the claims set forth in Appendix A below do not explicitly include the language submitted in the proposed amendment.

However, as discussed above, the amendment was proposed solely as clarification of the existing claim language. More specifically, those skilled in the art understand that passivation layers

inherently passivate or cover features thereunder except those features explicitly disclosed as exposed by the passivation layer. Accordingly, while the claim language of record explicitly recites "a passivation layer exposing only pads of the first set, or exposing pads of the first and second sets," it is implicit that the passivation layer inherently exposes only pads of the first set or only pads of the first and second sets.

V. SUMMARY OF THE INVENTION

The present invention provides an integrated circuit die having two sets of conductive pads formed thereon. A set of larger pads are suitable for flip-chip assembly and a set of smaller pads are suitable for wire bond assembly. A first predetermined center-to-center spacing between each pad of the first set and the adjacent pad or pads of the first set is larger than a second predetermined center-to-center spacing between each pad of the second set and the adjacent pad or pads of the first and second sets. The provision of pads complying with the minimum spacing requirements for both flip-chip and wire bond assembly enables a "dual purpose" (*e.g.*, one set of pads being for normal production and another set for testing purposes) die to be produced without any increase in die size. The integrated circuit die also includes a passivation layer exposing only pads of the first set, or exposing only pads of the first and second sets.

VI. ISSUES

A. Whether Claims 1-4 and 7-10, as rejected by the Examiner, are anticipated under 35 U.S.C. §102(e) by U.S. Patent No. 6,265,783 to Juso, *et al.* ("Juso").

B. Whether Claims 1-3 and 8-10, as rejected by the Examiner, are anticipated under 35 U.S.C. §102(b) by U.S. Patent No. 5,641,946 to Shim.

C. Whether Claim 7, as rejected by the Examiner, is unpatentable under 35 U.S.C. §103(a) in view of Shim.

VII. GROUPING OF THE CLAIMS

Claims 1-12 do not stand or fall together. Claims 1-7 form a first group of claims that stand or fall together, and Claims 8-12 form a second group of claims that stand or fall together.

VIII. SUMMARY OF REFERENCES RELIED ON BY THE EXAMINER

Juso is directed to a resin overmolded semiconductor device. (Column 3, lines 29-48). In that regard, and with reference to "Illustration 1" below which shows Juso's FIGs. 1 and 2, Juso discloses an insulating substrate 5 having through-holes 9 that expose underlying lands 10, dummy lands 11, a solder resist film 7 and an adhesive film 8, wherein the through-holes 9 allow the release of moisture through the insulating substrate 5 during a reflow process to prevent the semiconductor device 1 from swelling. (Fig. 1; column 5, lines 35-43). The dummy lands 11 may be constructed to cover or partially cover the through-holes in the insulative substrate 5. (Column 5, lines 40-44). Every land 10 and dummy land 11 is equidistant from adjacent lands 10 and dummy lands 11. (See, for example, FIGs. 2 and 4).

Fig. 1

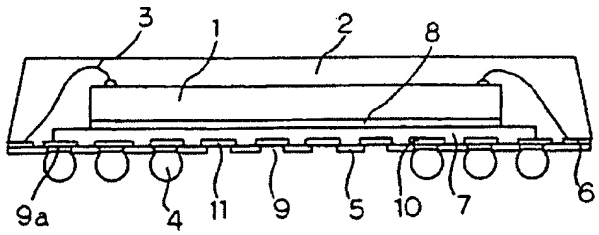

Fig. 2

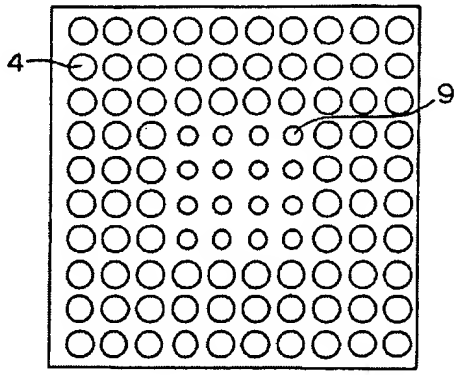

Illustration 1

Shim is directed to leveling the tops of solder balls which will be brought into contact with a mother board when a BGA semiconductor package is mounted to the mother board. (Column 2, lines 14-22). The tops of the solder balls are leveled by adjusting the size of solder ball lands used for welding the solder balls to the PCB, or by forming differently-sized exposed portions of solder ball lands using a mask after forming the solder ball lands. (Column 2, lines 23-28). In that regard, and with reference to "Illustration 2" below showing Shim's FIGs. 5A and 11, Shim discloses an

insulating layer 6 that exposes pads of three or four sets of conductive pads of respective heights h1, h2, h3 and H. (Column 5, lines 36-51; column 6, lines 42-56). Each pad includes a solder ball 3 and land 5. (See, for example, FIGs. 11 and 14). The center-to-center spacing between each pair of solder balls 3 is uniform across the PCB. (See FIGs. 5A, 6, 7, 9A, 10A, 12A and 13A).

FIG. 5A

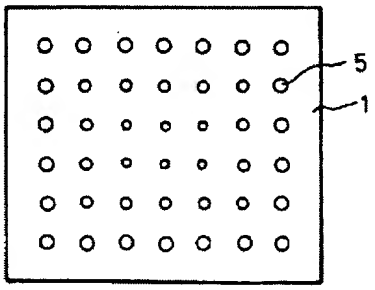

FIG. 11

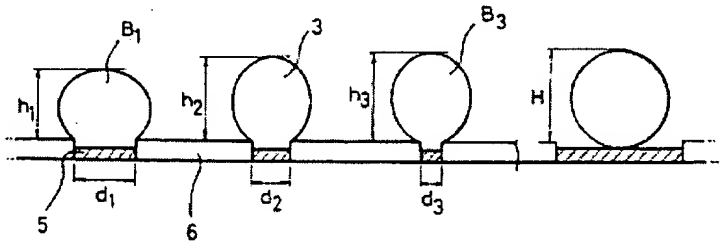

Illustration 2

IX. THE APPELLANTS' ARGUMENTS

Claims 1-12 do not stand or fall together. Claim 1 and its dependent Claims 2-7 form a first group of claims that stand or fall together. Claim 8 and its dependent Claims 9-12 form a second group of claims that stand or fall together. The Claims of the first and second groups are separately patentable.

Independent Claim 1 recites, among other elements, a first predetermined center-to-center spacing between each pad of a first set of pads and the adjacent pad or pads of the first set, and a second predetermined center-to-center spacing, less than said first spacing, between each pad of a second set and the adjacent pad or pads of the first and second sets. In contrast, Claim 8 recites, among other elements, a first set of conductive pads having a first minimum distance therebetween and a second set of conductive pads having a second minimum distance therebetween and between a pad of the second set and a neighboring pad of the first set. Thus, pads constructed according to Claim 1 are separated by one of two specific distances each having substantially no variation, whereas pads constructed according to Claim 8 merely require separation by one of two minimum distances, such that the pads constructed according to Claim 8 may be separated by distances substantially greater than one of the two minimum distances, whereas the spacing of pads constructed according to Claim 1 does not substantially vary. Therefore, the inventions recited in Claims 1 and 8 do not stand or fall together.

The inventions set forth in independent Claims 1 and 8 and their dependent claims are neither anticipated by nor obvious in view of Juso or Shim.

A. Rejection of Claims 1-4 and 7-10 under 35 U.S.C. §102(e) in view of Juso

Juso fails to anticipate Claims 1 and 8 and their dependent claims because Juso fails to disclose each and every element recited in Claims 1 and 8. For example, Juso fails to disclose a passivation layer that exposes only pads of a first set of conductive pads, or only pads of first and second sets of conductive pads, as recited in Claim 1 of the present application. In contrast, Juso discloses an insulating substrate 5 having through-holes 9 that expose underlying lands 10, dummy lands 11, a solder resist film 7 and an adhesive film 8, wherein the through-holes 9 allow the release of moisture through the insulating substrate 5 during a reflow process to prevent the semiconductor device 1 from swelling. (Fig. 1; column 5, lines 35-43). Because the insulating substrate 5 exposes the solder resist film 7 and the adhesive film 8, the insulating substrate 5 exposes more than the lands 10 and dummy lands 11. More specifically, the insulating substrate 5 doesn't expose only pads of a first set of conductive pads or only pads of first and second sets of conductive pads, as recited in Claim 1. Accordingly, Juso fails to anticipate the invention recited in Claim 1.

Moreover, because Juso explicitly provides openings in the insulating substrate 5 in order to release moisture during a reflow process to prevent the semiconductor device 1 from swelling, the insulating substrate 5 cannot be a passivation layer. A passivation layer would prevent such moisture release. In direct contrast, the Examiner asserts that the insulating substrate 5 functions as a protective or passivation layer. (Examiner's Action mailed June 4, 2002, pages 5-6). However, an insulating substrate (*e.g.*, the insulation substrate 5 in Juso) cannot function as a passivation layer if it includes holes through which moisture may travel. Those skilled in the art understand that a passivation layer is employed to passivate (*i.e.*, seal and otherwise prevent contamination or corrosion) a device or region thereof. Moreover, Juso also discloses that dummy lands 11 may be

constructed to only partially cover the through-holes in the insulative substrate 5, further reinforcing the fact that the insulative substrate 5 disclosed in Juso was not intended to be a passivation layer and, in fact, cannot even function as a passivation layer. Accordingly, the insulating substrate 5 disclosed in Juso is not a passivation layer. Consequently, Juso fails to disclose a passivation layer as recited in Claim 1 of the present application.

Furthermore, Juso fails to disclose a first predetermined center-to-center spacing between each pad of a first set and an adjacent pad or pads of the first set, and a second predetermined center-to-center spacing, less than the first spacing, between each pad of a second set and an adjacent pad or pads of the first and second sets, as recited in Claim 1. Juso also fails to disclose a first set of conductive pads having a first minimum distance therebetween, and a second set of conductive pads having a second minimum distance therebetween, and between a pad of the second set and a neighboring pad of the first set, as recited in Claim 8. In contrast, every land 10 and dummy land 11 disclosed in Juso is equidistant from adjacent pads. (See, for example, FIGs. 2 and 4). Because each land 10 and dummy land 11 is equidistant from an adjacent land 10 or dummy land 11, Juso fails to disclose sets of pads having first and second predetermined center-to-center spacings and first and second minimum distances therebetween.

Accordingly, Juso fails to disclose each and every element of Claims 1 and 8. Consequently, Juso is not an anticipating reference for Claims 1 and 8 and their dependent claims. Therefore, Claims 1-4 and 7-10 are not anticipated by Juso.

B. Rejection of Claims 1-3 and 8-10 under 35 U.S.C. §102(b) in view of Shim

Shim fails to anticipate Claims 1 and 8 and their dependent claims because Shim fails to disclose each and every element of Claims 1 and 8. More specifically, Shim fails to disclose a passivation layer that exposes only pads of a first set of conductive pads, or only pads of first and second sets of conductive pads, as recited in Claim 1 of the present application. In contrast, Shim discloses an insulating layer 6 that exposes more than pads of only a first set of conductive pads, or more than pads of first and second sets of pads. More specifically, Shim discloses that the insulating layer 6 exposes pads of three or four sets of conductive pads of respective heights h1, h2, h3 and H. (FIGs. 11 and 14).

Shim also fails to disclose that the center-to-center spacing of each set of pads differs between different sets of pads, as recited in Claim 1. Similarly, Shim also fails to disclose a first set of conductive pads having a first minimum distance therebetween, and a second set of conductive pads having a second minimum distance therebetween, and between a pad of the second set and a neighboring pad of the first set, as recited in Claim 8. In contrast, as clearly shown in FIGs. 5-14, Shim discloses that each solder ball 3 and land 5 are equidistant from adjacent solder balls 3 and lands 5. In other words, all of the figures in Shim depict all of the solder ball lands 5 and corresponding solder balls 3 as being uniformly spaced from one another, such that Shim fails to disclose a second spacing. Because the solder balls 3 and lands 5 are equidistant from all adjacent balls 3 and lands 5, they have the same center-to-center spacing instead of different center-to-center spacing. Similarly, because the solder balls 3 and lands 5 are equidistant from all adjacent balls 3 and lands 5, there is only a single minimum distance therebetween instead of first and second minimum distances.

In contrast, the Examiner asserts that if the spacing between the outermost lands 5 is defined as the first spacing of the first set, and the spacing between the innermost lands 5 is defined as the second spacing of the second set, then the spacing of the second set is clearly less than the first spacing of the first set because the innermost lands 5 are formed in the boundary of the outermost lands 5. (Examiner's Action, page 6). However, the Appellant believes the Examiner has inadvertently misinterpreted the claims of the present application. Specifically, Claim 1 recites a first predetermined center-to-center spacing between each pad of the first set and the adjacent pad or pads of the first set, and at least a second predetermined center-to-center spacing between each pad of the second set and the adjacent pad or pads of the first and second sets (Claim 8 contains a similar recitation). According to such a recitation, the center-to-center spacing is measured between each pad and an adjacent pad or pads. However, as clearly shown in FIGs. 9A and 11 of Shim, all of the lands 5 and solder balls 3 of equal size are equidistant from adjacent lands 5 or solder balls 3 of the same or different size. Thus, the outermost lands 5 have the same center-to-center spacing as the innermost lands 5. Accordingly, Shim fails to disclose that the center-to-center spacing of each set of pads differs between different sets of pads, as recited in Claim 1, and as similarly recited in Claim 8.

The Examiner has also asserted that the insulating mask 6 disclosed in Shim is a passivation layer as recited in Claims 1 and 8 of the present application. However, in the embodiments disclosed in Shim that include the insulating mask 6, the solder ball lands 5 all have the same size. Accordingly, Shim fails to disclose a single embodiment comprising both a passivation layer and first and second sets of conductive pads wherein the pads of the first set are larger than the pads of the second set, as recited in Claims 1 and 8 of the present application.

Accordingly, Shim fails to disclose each and every element of Claims 1 and 8. Consequently, Shim is not an anticipating reference for Claims 1 and 8 and their dependent claims. Accordingly, Claims 1-3 and 8-10 are not anticipated by Shim.

C. Rejection of Claim 7 under 35 U.S.C. §103(a) in view of Shim

As discussed above, Shim fails to teach a passivation layer that exposes only pads of a first set of conductive pads, or only pads of first and second sets of conductive pads, as recited in Claim 1 of the present application. Moreover, Shim fails to suggest such a passivation layer. In contrast, Shim teaches a passivation layer that exposes three or four sets of conductive pads, as discussed above.

Shim also fails to teach sets of conductive pads having different predetermined center-to-center spacing, as also discussed above. Moreover, Shim fails to suggest such conductive pads. In contrast, Shim merely teaches that all solder balls 3 and lands 5 are equidistant from adjacent solder balls 3 and lands 5, such that there are no sets of pads discernible by a unique center-to-center spacing different from that of another set of pads.

Accordingly, Shim fails to teach or suggest each and every element of Claim 1 of the present application. Therefore, Shim fails to support a *prima facie* case of obviousness with respect to Claim 1 and its dependent Claims. Consequently, Claim 7 is not obvious in view of Shim.

For the reasons set forth above, the Claims on appeal are patentable over the Juso and Shim references relied upon by the Examiner. Accordingly, the Appellants respectfully request that the

Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of the Appellants' pending Claims 1-4 and 7-10.

Respectfully submitted,

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Dated: 12/4/02

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X. APPENDIX A - CLAIMS

1. An integrated circuit die including first and second sets of conductive pads for enabling external connections to be made to the integrated circuit, wherein each pad of said first set is larger than each pad of said second set, there being at least a first predetermined center-to-center spacing between each pad of the first set and the adjacent pad or pads of the first set, and at least a second predetermined center-to-center spacing, less than said first spacing, between each pad of the second set and the adjacent pad or pads of the first and second sets, and a passivation layer exposing only pads of the first set, or exposing pads of the first and second sets.

2. A die as claimed in claim 1 wherein the pads of the first set are larger in area than the pads of the second set.

3. A die as claimed in claim 2 wherein the area of each pad of the first set and the first predetermined center-to-center spacing are suitable for flip-chip assembly of the die, and the area of each pad of the second set and the second predetermined center-to-center spacing are suitable for wire bond assembly of the die.

4. A die as claimed in claim 1 wherein the pads of the first and second sets are disposed in line adjacent one or more edges of the die.

5. A die as claimed in claim 1 wherein the pads of the first set are disposed in two lines adjacent one or more edges of the die, the pads of the first set in one of the two lines being disposed in staggered relationship with respect to the pads of the first set in the other of the two lines.

6. A die as claimed in claim 5 wherein the pads of the second set are disposed in one of the two lines.

7. A die as claimed in any preceding claim wherein the first set of pads is connected to one set of connection points in the integrated circuit, and the second set of pads is connected to another set of connection points in the integrated circuit.

8. An integrated circuit die, comprising:

a first set of conductive pads having a first minimum distance therebetween; and

a second set of conductive pads having a second minimum distance therebetween, and between a pad of the second set and a neighboring pad of the first set, wherein each pad of said first set is larger than each pad of said second set;

wherein the die is adapted for selective use as one of a flip-chip assembly and a wire bond.

9. A die as recited in claim 8, further comprising a first passivation layer for use of the die as a flip-chip assembly.

10. A die as recited in claim 8, further comprising a passivation layer for use of the die as a wire bond assembly.

11. An integrated circuit die including first and second sets of conductive pads for enabling external connections to be made to the integrated circuit, there being at least a first predetermined center-to-center spacing between each pad of the first set and the adjacent pad or pads of the first set, and at least a second predetermined center-to-center spacing, less than said first spacing, between each pad of the second set and the adjacent pad or pads of the first and second sets, wherein the pads of the first set are disposed in two lines adjacent one or more edges of the die, the pads of the first set in one of the two lines being disposed in staggered relationship with respect to the pads of the first set in the other of the two lines, and a passivation layer exposing only pads of the first set, or exposing pads of the first and second sets.

12. A die as claimed in Claim 11 wherein the pads of the second set are disposed in one of the two lines.

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STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Agere Systems Inc.

Application No./Patent No.: 09/639,288 Filed/Issue Date: August 15, 2000

Entitled: INTEGRATED CIRCUIT DIE FOR WIRE BONDING AND FLIP-CHIP MOUNTING

Agere Systems Inc., a corporation,
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

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REEL/FRAME: 012722/0926
NUMBER OF PAGES: 4

BRIEF: ASSIGNMENT OF ASSIGNOR'S INTEREST (SEE DOCUMENT FOR DETAILS).

ASSIGNOR:
ADDINALL, ROSS

DOC DATE: 02/27/2002

ASSIGNOR:
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DOC DATE: 02/25/2002

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SERIAL NUMBER: 09639288
PATENT NUMBER:

FILING DATE: 08/15/2000
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Second Party

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Name (line 2):

Receiving Party

[ ] Mark if additional names of receiving parties attached

Name (line 1): Agere Systems Guardian Corporation

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Month	Day	Year
02	27	2002

Patent Cooperation Treaty (PCT)

Enter PCT application number only if a U.S. Application Number has not been assigned.

PCT ____ PCT ____ PCT ____

PCT ____ PCT ____ PCT ____

Number of Properties

Enter the total number of properties involved. # 1

Fee Amount

Fee Amount for Properties Listed (37 CFR 3.41): $ 40.00

Method of Payment: Deposit Account

Enclosed ☒ Deposit Account ☐

(Enter for payment by deposit account or if additional fees can be charged to the account.)

Deposit Account Number: #

Authorization to charge additional fees: Yes ☐ No ☐

Statement and Signature

To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document. Charges to deposit account are authorized, as indicated herein.

Greg H. Parker		03/07/2002
Name of Person Signing	Signature	Date

DOCKET NO. R. ADDINALL 1-1 PATENT

ASSIGNMENT

WHEREAS, We, Ross Addinall, a citizen of Great Britain and resident of Tadley, Hampshire, and Gareth Rhys Davies, a citizen of Great Britain and resident of East Garston, Berkshire, have invented certain new and useful improvements in "Improvements in or relating to Integrated Circuit Dies" for which we filed an application for United States Letters Patent on August 15, 2000, Serial No. 09/639,288; and

WHEREAS, Agere Systems Guardian Corporation, a corporation of the State of Delaware, having offices at 9333 S. John Young Parkway, Room 301E1211, Orlando, Florida, 32819, U.S.A., (hereinafter referred to as "ASSIGNEE"), is desirous of acquiring my entire right, title and interest in and to the invention, and in and to the said application and any Letters Patent that may issue thereon;

NOW, THEREFORE, for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, I do hereby sell, assign and transfer unto said ASSIGNEE, its successors, assigns and legal representatives, the full and exclusive right, title and interest in and to said invention and in and to said application and all patents which may be granted therefor, and all divisions, reissues, substitutions, continuations, continuations-in-part and extensions thereof; and I hereby authorize and request the Commissioner of Patents and Trademarks to issue all patents for said invention, or patents resulting therefrom, insofar as my interest is concerned, to the said ASSIGNEE of my entire right, title and interest.

I also hereby sell and assign to said ASSIGNEE, its successors, assigns and legal representatives the full and exclusive rights, title and interest to the invention disclosed in said application throughout the world, including the right to file applications and obtain patents, utility models, industrial models and designs for said invention in its own name throughout the world including all rights of priority, all rights to publish cautionary notices reserving ownership of said invention and all rights to register said invention in appropriate registries; and I further agree to execute any and all powers of attorney, applications, assignments, declarations, affidavits, and any other papers in connection therewith necessary to perfect such rights, title and interest in ASSIGNEE, its successors, assigns and legal representatives.

I hereby further agree that I will communicate to said ASSIGNEE, or to its successors, assigns and legal representatives, any facts known to us respecting any improvements; and, at the expense of said ASSIGNEE, to testify in any legal proceedings, sign all lawful papers, execute all divisional, continuation, continuation-in-part, reissue and substitute applications, and make all

lawful oaths, and generally do everything possible to vest title in said ASSIGNEE and to aid said ASSIGNEE, its successors, assigns and legal representatives to obtain and enforce proper protection for said invention in all countries.

R. Addinall

Ross Addinall

TOWN: Tadley

COUNTRY: United Kingdom

On this 27 day of February, 2002, before me personally came Ross Addinall, to me known to be the individual described herein and who executed the foregoing instrument, and acknowledged execution of the same.

Paul B

Witness

Gareth Rhys Davies

TOWN: EAST GARSTON

COUNTRY: UK

On this 25th day of February, 2002, before me personally came Gareth Rhys Davies, to me known to be the individual described herein and who executed the foregoing instrument, and acknowledged execution of the same.

Witness

STATE OF DELAWARE
SECRETARY OF STATE
DIVISION OF CORPORATIONS
FILED 09:00 AM 08/29/2002
020545223 - 3268412

CERTIFICATE OF OWNERSHIP AND MERGER

OF

Agere Systems Guardian Corp.
(a Delaware corporation)

INTO

Agere Systems Inc.
(a Delaware corporation)

UNDER SECTION 253 OF THE GENERAL CORPORATION LAW OF THE STATE OF DELAWARE

Agere Systems Inc., a corporation organized and existing under the laws of Delaware ("Corporation"), **DOES HEREBY CERTIFY:**

FIRST: The Corporation is the owner of all of the outstanding shares of common stock of Agere Systems Guardian Corp., which is also a business corporation of the State of Delaware.

SECOND: On August 22, 2002 the Subsidiary Governance Committee of the Board of Directors of the Corporation adopted the following resolution to merge Agere Systems Guardian Corp. into the Corporation:

> **RESOLVED** that Agere Systems Guardian Corp., a Delaware corporation, shall be merged with and into Agere Systems Inc., a Delaware corporation, with Agere Systems Inc. being the surviving corporation, and Agere Systems Inc. shall thereupon assume all of the obligations of Agere Systems Guardian Corp."

THIRD: That the merger authorized hereby shall become effective as of 9:00 a.m. Eastern Standard Time on August 31, 2002.

Executed on August 22, 2002

AGERE SYSTEMS INC.

By Paul Bento
Paul Bento, Vice President

Delaware

The First State

I, HARRIET SMITH WINDSOR, SECRETARY OF STATE OF THE STATE OF DELAWARE, DO HEREBY CERTIFY THE ATTACHED IS A TRUE AND CORRECT COPY OF THE CERTIFICATE OF OWNERSHIP, WHICH MERGES:

"AGERE SYSTEMS GUARDIAN CORP.", A DELAWARE CORPORATION,

WITH AND INTO "AGERE SYSTEMS INC." UNDER THE NAME OF "AGERE SYSTEMS INC.", A CORPORATION ORGANIZED AND EXISTING UNDER THE LAWS OF THE STATE OF DELAWARE, AS RECEIVED AND FILED IN THIS OFFICE THE TWENTY-NINTH DAY OF AUGUST, A.D. 2002, AT 9 O'CLOCK A.M.

AND I DO HEREBY FURTHER CERTIFY THAT THE EFFECTIVE DATE OF THE AFORESAID CERTIFICATE OF OWNERSHIP IS THE THIRTY-FIRST DAY OF AUGUST, A.D. 2002.

A FILED COPY OF THIS CERTIFICATE HAS BEEN FORWARDED TO THE NEW CASTLE COUNTY RECORDER OF DEEDS.

Harriet Smith Windsor

Harriet Smith Windsor, Secretary of State

3268412 8100M

020545223

AUTHENTICATION: 1959517

DATE: 08-29-02